REMARKS

Claims 1 - 45 are pending in the above-identified application. Claims 1 - 19 are withdrawn from consideration.

In the Office Action of May 22, 2002, Claims 20 - 45 were rejected. No claim was allowed. In response, Claim 20 is amended and Claims 36 and 39 - 41 are canceled. Reexamination and reconsideration are respectfully requested in view of the foregoing amendments and the following remarks.

Objections to the Claims

In Claim 20, the Examiner requests that "chip" in line 3 be changed to "substrate". In response, Claim 20 is amended as suggested by the Examiner. Accordingly, it is respectfully submitted that this objection is overcome.

Rejection of Claims 20 - 45 under 35 U.S.C. §112, second paragraph

Claims 20 - 45 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. In particular, the Examiner alleges that: no method steps are recited in Claim 20.

In response, Claim 20 is amended to recite method steps.

Accordingly, it is respectfully submitted that the rejection of Claim 20 under 35 U.S.C. §112, second paragraph, is thereby overcome.

Rejection of Claims 20, 22, 31 - 34 and 42 under 35 U.S.C. §102(e) over Maikawa

Claims 20, 22, 31 – 34 and 42 are rejected under 35 U.S.C. §102(e) as being anticipated by Maekawa (U.S. Patent No. 6,171,957).The Examiner alleges that

Maekawa discloses the claimed method of fabricating a semiconductor integrated circuit device

This rejection is respectfully traversed as it may apply to the amended claims. In the first place, although Maekawa mentions the purity of copper in the sputtering target, the reference does not contain any teaching or suggestion regarding the purity of copper wiring in the finished device. Moreover, independent Claim 20 of the present invention is amended herein to provide that the film thickness of the thinnest part of the conducting barrier film in the side walls of the embedded interconnection slot and the connecting hole is less than 10 nm. This feature is neither disclosed nor suggested by Maekawa, which discloses only damascene type interconnections without conducting barriers and with relatively thick barriers and does not disclose or suggest thin conducting barriers. Moreover, although Maekawa mentions the purity of copper in the sputtering target, the reference does not contain any teaching or suggestion regarding the purity of copper wiring in the finished device.

Accordingly, it is respectfully submitted Claims 20, 22, 31 – 34 and 42 are not anticipated by or obvious over Maekawa.

Rejection of Claims 21, 23, 28 - 31, 35 - 41 and 43 - 45 under 35 U.S.C. §103(a) over Maikawa

Claims 21, 23, 28 – 31, 35 – 41 and 43 – 45 are rejected under 35 U.S.C. §103(a) as obvious over Maekawa. Regarding Claims 21 and 23, the Examiner alleges that Maekawa discloses copper purity of 99.999% and that it would be obvious to provide copper purity of 99.9999%. Regarding Claim 28, the Examiner alleges that Maekawa discloses performing CMP to the first metal film. The Examiner acknowledges that the reference does not disclose abrasive particle-free CMP, but

the Examiner takes the position that it would have been obvious to do so to prevent damage to the film. Regarding Claims 29 - 31, 35 - 41 and 43 - 45, the Examiner takes the position that it would have been obvious to form the conducting barrier film, the concentration of other components in copper, the mass ratio of abrasive particles, the width of the embedded interconnection slot, having a desired thickness, concentration, ratio and height on the alleged grounds that discovering an optimum value of a result effective variable involves only routine skill in the art.

This rejection is respectfully traversed. As discussed above, amended independent Claim 20 requires that the film thickness of the thinnest part of the conducting barrier film in the side walls of the embedded interconnection slot and the connecting hole be less than 10 nm. This feature is neither disclosed nor suggested by Maekawa, which discloses only damascene type interconnections without conducting barriers and with relatively thick barriers and does not disclose or suggest thin conducting barriers.

Accordingly, it is respectfully submitted that Claims 21, 23, 28 – 31, 35 – 41 and 43 – 45 are not anticipated or obvious over Maekawa.

Rejection of Claims 24 - 27 under 35 U.S.C. §103(a) over Maikawa in view of Ngo

Claims 24 - 27 are rejected under 35 U.S.C. §103(a) as obvious over Maekawa in view of Ngo et al (U.S. Patent No. 6,348,410). The Examiner alleges that Maekawa discloses a metal film planarized by chemical mechanical polishing. The Examiner acknowledges that Maekawa does not disclose the first main surface of the semiconductor substrate is plasma treated in an atmosphere of a gas having reducing properties prior to forming a cap insulating film. The Examiner alleges that

Ngo discloses forming a metal film planarized by chemical mechanical polishing and a first main surface of the semiconductor substrate plasma treated in an atmosphere of a gas having reducing properties prior to forming a cap insulating film. The Examiner takes the position that it would have been obvious to plasma treat the first main surface of the semiconductor substrate of Maekawa in an atmosphere of a gas having reducing properties prior to forming a cap insulating film. The Examiner takes the position that it would have been obvious to treat the first main surface of the semiconductor substrate of Maekawa in an atmosphere of a gas having reducing properties prior to forming a cap insulating film in order to suppress hillocks formation.

This rejection is respectfully traversed. Ngo discloses only ammonia plasma treatment just before cap SiN plasma deposition. Ngo does not disclose or suggest a thin conducting barrier (less than 10 nm) as presently required by independent Claim 20. As discussed above, this feature is not disclosed or suggested by Maekawa either.

Accordingly, it is respectfully submitted that if Claims 24 - 27 are not obvious over Maekawa and Ngo, alone or in combination.

Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that Claims 20 - 35, 37 - 38 and 42 - 45 are in condition for allowance. Favorable reconsideration is respectfully requested.

Should the Examiner believe that anything further is necessary to place this application in condition for allowance, the Examiner is requested to contact applicants' undersigned attorney at the telephone number listed below.

Kindly charge any additional fees due, or credit overpayment of fees, to Deposit Account No. 01-2135 (501.39932X00).

Respectfully submitted,

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By_____
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RTW/dlt

Attachment: Marked-up version showing changes made

MARKED UP VERSION TO SHOW CHANGES MADE

IN THE CLAIMS:

20. (Amended) A method of fabricating a semiconductor integrated circuit device comprising:

(a) providing a semiconductor ~~chip~~ substrate having a first main surface,

(b) forming a first insulating film ~~formed~~ over said first main surface of said semiconductor substrate,

(c) forming an embedded interconnection slot ~~formed~~ over said first insulating film main surface,

(d) forming a connecting hole ~~provided~~ in a bottom surface of said embedded interconnection slot, and connected to a lower conducting layer,

(e) forming a conducting barrier film ~~formed~~ over surface region of the bottom surface and side surface of said embedded interconnection slot and said connecting hole,

(f) forming an embedded metal interconnection layer having copper as its main component embedded in said interconnection slot and in said connecting hole in which said conducting barrier film is formed, and

(g) forming a cap insulating film ~~formed~~ so as to cover said embedded metal interconnection layer and the upper surface of said first insulating film, wherein:

the concentration of components other than copper in said embedded metal interconnection layer in the finished semiconductor ~~chip~~ integrated circuit device does not exceed 0.8At%, and

~~the purity of copper in the metal film when an embedded metal film having copper as its principal component is formed to form said embedded metal interconnection layer, is not less than 99.999%~~ the film thickness of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is less than 10 nm.